CLAIMS

What is claimed is:

1. An integrated circuit comprising:

switching logic; and

a control interface having:

a first interface for connection to an interchangeable one of a first bus of a first processor and a first and second bus of a second processor,

a second interface for connection to a data bus and an address bus of said switching logic, and

selection logic coupled to said first and second interfaces and equipped to receive a control signal identifying one of a first control mode to couple said first bus of said first processor to both said data bus and said address bus of said switching logic, and a second control mode to couple said first bus of said second processor to said data bus of said switching logic and to couple said second bus of said second processor to said address bus of said switching logic.

2. The integrated circuit of claim 1, wherein said control interface operates in said first control mode when said first interface is coupled to a multiplexed address and data bus of said first processor.

3. The integrated circuit of claim 1, wherein said control interface operates in said second control mode when said first interface is coupled to separate address and data buses of said second processor.

4. The integrated circuit of claim 1, further comprising:

delay circuitry to programmably delay transmission of an address from one of said first and second processors to said address bus of said switching logic.

5. The integrated circuit of claim 1, further comprising:

a read data bus coupled to said first interface and said second interface to transmit multiplexed data and address signals between said switching logic coupled to said second interface and said first processor coupled to said first interface when said control signal identifies said first control mode, and to transmit data signals between said switching logic coupled to said second interface and said second processor coupled to said first interface when said control signal identifies said second control mode.

6. The integrated circuit of claim 1, wherein said control signal is received from an identified on of said first processor and said second processor.

7. A control interface for transmitting signals between an integrated circuit and an identifiable one of at least a first processor type operating in accordance with a

first protocol and a second processor type operating in accordance with a second protocol, comprising:

a first signal path to couple one of a first bus of said first processor type and a second bus of said second processor type, with a data bus of said integrated circuit based at least in part upon an identified processor type;

a second signal path to couple said first bus of said first processor type with an address bus of said integrated circuit;

a third signal path to couple a third bus of said second processor type with said address bus of said integrated circuit; and

selection logic to select between said second and said third signal paths based at least in part upon said identified processor type.

8. The control interface of claim 7, wherein if said selection logic selects said second signal path then said third signal path is not utilized.

9. The control interface of claim 8, further comprising:

identification logic to identify which of said first processor type and said second processor type is coupled to said control interface.

10. The control interface of claim 7, wherein said first signal path transmits data signals to said integrated circuit, and said second and third signal paths transport address signals to said integrated circuit.

11. A control interface to be coupled to and transmit signals between a logic device and at least one of a first processor operating in accordance with a first protocol and a second processor operating in accordance with a second protocol, comprising:

a first signal line to receive a read strobe signal and a transfer start indication signal;

a second signal line to receive a write strobe signal and a read/write indicator signal to indicate read/write transactions;

first selection logic to signal a write transaction to said logic device if said control interface is coupled to said first processor and said write strobe signal is received on said second signal line, or said control interface is coupled to said second processor and a transfer start indication signal is received on said first signal line and a write transaction is indicated by said read/write indicator signal on said second signal line; and

second selection logic to signal a read transaction to said logic device if said control interface is coupled to said first processor and said read strobe signal is received on said first signal line, or said control interface is coupled to said second processor and a transfer start indication signal is received on said first signal line and a read transaction is indicated by said read/write indicator signal on said second signal line.

12. The control interface of claim 11, further comprising:

indicator logic coupled to said first selection logic and said second selection logic to identify whether said control interface is coupled to said first processor or said second processor.

13. The control interface of claim 11, further comprising:

programmable delay circuitry to dynamically delay said write transaction.

14. The control interface of claim 13, wherein said programmable delay circuitry comprises circuitry to delay said write transaction from one to three clock cycles based at least in part upon timing requirements of said first or second processor.

15. An apparatus comprising:

a first interface to couple said apparatus to one of a plurality of host devices and a second interface to couple said apparatus to a second device,

said first interface being equipped to interchangeably receive either multiplexed address and data signals from a first bus of a first host device of said plurality of host devices for transmission to an address bus and a data bus of said second device, or address signals from a second bus of a second host device of said plurality of host devices for transmission to said address bus of said second device and data signals from a third bus of said second host device for transmission to said data bus of said second device; and

said first interface being further equipped to receive one or more control signals including a read strobe signal and a write strobe signal if said apparatus is coupled to one of said plurality of host devices operating in accordance with a first protocol, and to receive one or more control signals including a transfer start indication signal and a read/write indicator signal if said apparatus is coupled to one of said plurality of host devices operating in accordance with a second protocol.

16. The apparatus of claim 15, wherein said first interface is equipped to interchangeably coupled said apparatus to one of a plurality of microprocessors.

17. The apparatus of claim 15, further comprising:

first delay circuitry to programmably delay address signals to be transmitted to said address bus of said second device; and

second delay circuitry to programmably delay write transactions to be transmitted to said second device.

18. The apparatus of claim 17, wherein said first and second delay circuitry is programmed to delay said address signals and said write transactions based at least in part upon operating characteristics of a host device coupled to said first interface.

19. The apparatus of claim 18, wherein said first delay circuitry and said second delay circuitry are programmed to delay an equal number of clock cycles.

20. A microprocessor comprising:

internal resources; and

interface logic to selectively couple said microprocessor to an interchangeable one of a plurality of host microprocessors including a first host microprocessor having a first architecture type and a second host microprocessor having a second architecture type to provide a selected one of said first and second host microprocessors with access to said resources.